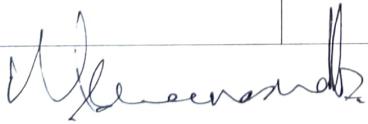
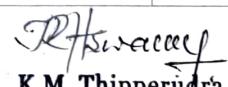


**ACADEMIC PLANNER**  
**DEPARTMENT OF ELECTRONICS**  
**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR II STAGE, BENGALURU-55.**

NAME: Prof. Thipperudra Swamy K.M. HOD of Electronics.  
(I, III & V Semesters for the Academic Year 2020-21) Reopen – 01/09/2020

| Class         | September   | October   | November   | December  |
|---------------|---|---|--|---|
| I Sem B.Sc.   | <b>UNIT-1:</b> DC and AC response of RC & RL Circuits, Transformer, switches.(10H)<br><b>UNIT-2:</b> Networks Theorems (DC analysis) KCL, KVL, open and short circuits, Voltage and current divider theorems. Star- Delta Conversion. Thevenin's & Superposition theorems. (6H) | <b>UNIT-2:</b> Maximum power transfer & Reciprocity theorems. (2H)<br><b>UNIT-3:</b> Semiconductor Diode and its applications. HWR & FWR. Filter. Zener diode Regulator. IC Regulators. (12H)<br>Internal Test. | <b>UNIT-4:</b> BJT-Construction, working, biasing and characteristics. BJT Biasing and circuits.<br>FET- Construction, characteristics and parameters. (14H)                             | <b>UNIT-5:</b> Number systems and Interconversions. Codes- BCD, Gray, and excess-3 codes. ASCII and EBCDIC codes. Numerical problems. (8H)<br>Test and Assignments.       |
| III Sem B.Sc. | <b>UNIT-3:</b> C Programming- Introduction, structure, operators, evaluation of expressions, Arrays, Programs. (8H)   | <b>UNIT-3:</b> Input and Output statements, library functions, programs. (4H)<br><b>UNIT-4:</b> Decision making, branching and looping- (4H)<br>Internal test.  | <b>UNIT-4:</b> for loop, do loop, while loop, function arguments and passing, programs. (4H)<br><b>UNIT-5:</b> Defining, declaring and initializing structure, arrays of structure. (4H) | <b>UNIT-5:</b> structure and functions, unions. Examples (4H)<br>Test and Assignments.  |
| V Sem B.Sc.   | <b>UNIT-1:</b> Introduction to Microprocessor- Features, different buses, addressing modes, Instruction set, T states, Delay ops, Numerical examples. (12H)   | <b>UNIT-2:</b> Stack operations, subroutine calls and returns, Assembly level Programs of various operations. Interrupts, and basic interfacing concepts. Internal test. (12H)                                  | <b>UNIT-3:</b> I/O instructions and Interfacing- Memory interfacing, i/o interfacing concepts, key board and LED interfacing. (2H)<br>Antennas: Full unit (8H)                           | <b>Unit-5:</b> Television- Introduction, Scanning, TV standards, monochrome TV transmitter and receiver, Color TV concepts and numerical problems. (8H)<br>Internal test. |

  
**PRINCIPAL**  
**VIVEKANANDA DEGREE COLLEGE**  
**BENGALURU-55**

  
**K.M. Thipperudra Swamy**  
**HOD of Electronics**  
**Vivekananda Degree College**  
**Rajajinagar, Bangalore - 560 055**

**ACADEMIC PLANNER**  
**DEPARTMENT OF ELECTRONICS**

VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR II STAGE, BENGALURU-55.

NAME: Prof. Thipperudra Swamy K.M. HOD of Electronics.

( VI Semesters for the Academic Year 2020-21) Reopen - 03.05.2021 ( Online classes only )

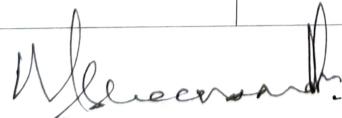
| Class        | May  | June  | July  |
|--------------|--|---|---|
| VI Sem B.Sc. | <b>UNIT-1:</b> Introduction to Microcontroller-Types, Architecture, Registers, Counters and timers, TCON, SCON, PCON, (10H)<br>Interrupts-IE, IP. (2H) | <b>UNIT-2:</b> Addressing modes, Instruction set,<br>Assembly level Programs of various operations. (8H)<br>Jump & Call instructions, simple programs. (3H)<br>Internal Test. | <b>UNIT-3:</b> 8051 programming using C, Timer/Counter programming, Example programs. (6H)<br><b>UNIT-4:</b> Interfacing with 8051-Keyboard , seven segment display. (6H) |

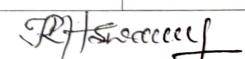
PRINCIPAL  
**VIVEKANANDA DEGREE COLLEGE**  
**BENGALURU-55**

K.M. Thipperudra Swamy  
 HOD of Electronics  
 Vivekananda Degree College  
 Rajajinagar, Bangalore - 560 055

**ACADEMIC PLANNER**  
**DEPARTMENT OF ELECTRONICS**  
**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR II STAGE, BENGALURU-55.**  
**NAME: Prof. Thipperudra Swamy K.M. HOD of Electronics.**  
**(II, IV & VI Semesters for the Academic Year 2020-21) Reopen – 26/07/2021**

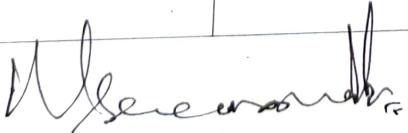
| Class        | July  | August  | September   | October  |
|--------------|---|---|---|--|
| II Sem B.Sc. | <b>UNIT-1:</b> Small Signal Amplifier-CE Amplifier, derivation for Av, Swamped Amplifier.<br><br>(4H)   | Multistage Amplifier, Darlington Amplifier and JFET Amplifier. (8H)<br><b>UNIT-2:</b> Power and Tuned Amplifier- Classification, class A power amplifier, Class B push pull power Amplifier, tuned amplifiers.<br>Internal test. (8H) | <b>UNIT-3:</b> Differential Amplifier- derivation for q point, Current mirror. (8H)<br><b>UNIT-4:</b> Concept, effect of negative FB. Oscillators- Types, circuits, working and expressions . (8H)                        | Multivibrators, numerical problems. (2H)<br><b>UNIT-5:</b> MOSFET- Working & characteristics. UJT, SCR, LED and LCD – Construction, working and characteristics. (14H) |
| IV Sem B.Sc. | <b>UNIT-1:</b> Boolean algebra, SOP & POS. Basic logic gates. (2H)  | Universal property of NAND & NOR Gates, K map, TTL NAND gate, CMOS inverter.<br>(8H)<br>Internal test.  | <b>UNIT-2:</b> Combinational logic circuits-HA, FA, HS, FS, encoder, decoder, multiplexer, demultiplexer, A-D & D-A Conversion.<br>Successive approximation ADC. (10H)  | <b>UNIT-3:</b> Flip flops, Registers and counters. Design of synchronous counter using K Map. (8H)   |
| VI Sem B.Sc. | <b>Revision</b><br><b>UNIT-1:</b> Introduction to Microcontroller- Types, Architecture, Registers. Memory organization of 8051. counters & timers, TCON, TMOD, SCON & PCON.<br><br>(3H) | <b>Revision</b><br><b>UNIT-2:</b> Interrupts, addressing modes, Data transfer instructions, Examples. Logical & arithmetic instructions, ALP.<br><b>UNIT-3:</b> Jump & Call instructions, (12H)                                       | <b>Revision</b><br>simple programs. 8051 programming using C.(8H)<br>Internal test. <b>Unit-4:</b> Basic interfacing concepts, interfacing of 8051 to keyboard, stepper motor, DAC, ADC & Traffic light controller. (12H) |  |

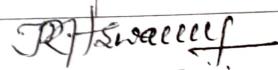
  
**PRINCIPAL**  
**VIVEKANANDA DEGREE COLLEGE**  
**BENGALURU-55**

  
**K.M. Thipperudra Swamy**  
**HOD of Electronics**  
**Vivekananda Degree College**

**ACADEMIC PLANNER**  
**DEPARTMENT OF ELECTRONICS**  
**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR II STAGE, BENGALURU-55.**  
**NAME: Prof. Thipperudra Swamy K.M. HOD of Electronics.**  
**(I, III & V Semesters for the Academic Year 2019-20)      Reopen - 8.7.2019**

| Class         | July   | August  | September   | October  |
|---------------|--|---|---|--|
| I Sem B.Sc.   | <b>UNIT-1:</b> DC and AC response of Electronic passive components. (10H)<br><br><b>UNIT-2:</b> Networks Theorems (DC analysis) KCL, KVL, (2H) | <b>UNIT-2:</b> open and short circuits, Voltage and current divider theorems. Networks Theorems- Thevenin's, Norton's, and Superposition Theorems. (7H)<br><br><b>UNIT-3:</b> RPS, HWR, FWR, Filters (9H)<br><br>Internal Test. | Zener diode & Transistor series. regulator. (4H)<br><br><b>UNIT-4:</b> BJT and FET- Working, biasing, Characteristics, Types of biasing circuits, Transistor as a switch. (12H) | JFET-Working, parameters, comparision with BJT.<br><br><b>UNIT-5:</b> Number systems and codes- Number systems and inter conversion. BCD, Gray, and excess-3 codes. ASCII and EBCDIC codes. (13H)<br><br>Test and Assignments. |
| III Sem B.Sc. | <b>UNIT-3:</b> C Programming- Introduction, structure, operators, evaluation of expressions, Arrays, (6H)                                      | <b>UNIT-3:</b> Input and Output statements, library functions, programs. (4H)<br><br><b>UNIT-4:</b> Decision making, branching and looping- (4H)<br><br>Internal test.  | <b>UNIT-4:</b> for loop, do loop, while loop, function arguments and passing, programs. (4H)<br><br><b>UNIT-5:</b> Structures and unions- (4H)                                  | Structures and unions: Arrays of structure, structure and functions, examples. (6H)<br><br>Test and Assignments.   |
| V Sem B.Sc.   | <b>UNIT-1:</b> Introduction to Microprocessor- Features, different buses, addressing modes, Instruction set, T states, Delay oops, (9H)        | <b>UNIT-2:</b> Examples on delay loops Stack operations, subroutine calls and returns, Assembly level Programs of various operations. Interrupts, and basic interfacing concepts. Internal test. (12H)                          | <b>UNIT-3:</b> I/O instructions and Interfacing- Memory interfacing, i/o interfacing concepts, key board and LED interfacing. (4H)<br><br>Antennas: Full unit (8H)              | <b>Unit-5:</b> Television- Introduction, Scanning, TV standards, monochrome TV transmitter and receiver, Color TV concepts and numerical problems. (8H)<br><br>Internal test.  |

  
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**K.M. Thipperudra Swamy**  
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Rajajinagar, Bangalore - 560 055

**ACADEMIC PLANNER**  
**DEPARTMENT OF ELECTRONICS**  
**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR II STAGE, BENGALURU-55.**

NAME: Prof. Thipperudra Swamy K.M. HOD of Electronics.

(II, IV & VI Semesters for the Academic Year 2019-20) Reopen - 09.01.2020

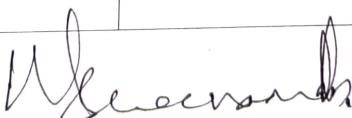
| Class        | January   | February  | March  | April   |
|--------------|---|---|--|---|
| II Sem B.Sc. | UNIT-1: Small Signal Amplifier-CE Amplifier, Swamped Amplifier, Multistage Amplifier, Darlington Amplifier and JFET Amplifier.<br><br>(12H)         | UNIT-2: Classification, class A ,Class B power amplifier and tuned amplifiers- (9H)<br><br>UNIT-3: Differential Amplifier- derivation for q point, (7H)<br><br>Internal test. | Current mirror- Circuit and working<br><br>UNIT-4: Effect of -ve FB, Expressions and numerical problems. Oscillators- circuits, Multivibrators,numerical problems. (14H) | UNIT-5:MOSFET, UJT, SCR, LED and LCD – Construction, working and characteristics. Triac and Diac- Symbol, features, operation and applications. (14H)<br><br>Internal test and assignments. |
| IV Sem B.Sc. | UNIT-1: Boolean algebra, SOP & POS. Basic logic gates. Universal property of NAND & NOR Gates, K map, TTL NAND gate. (6H)                           | CMOS inverter.<br><br>UNIT-2: Combinational logic circuits-HA, FA, HS, FS, Encoder, Decoder, Multiplexer, Demultiplexer. (8H)   | A-D & D-A Conversion. Successive approximation ADC.<br><br>UNIT-3: Flip flops, Registers and counters. Design of synchronous counter using K Map. (8H)                   | Programmable Logic Devices- SPLDs, ROM, PLA and GAL. CPLD and FPGA. (6H)  |
| VI Sem B.Sc. | UNIT-1: Introduction to Microcontroller-Types, Architecture, Registers, Counters and timers, TCON, SCON, PCON, (10H)<br><br>Interrupts-IE, IP. (2H) | UNIT-2:Addressing modes, Instruction set, Assembly level Programs of various operations. (8H)<br><br>Jump & Call instructions, simple programs. (3H)<br><br>Internal Test.    | UNIT-3: 8051 programming using C, Timer/Counter programming, Example programs. (6H)<br><br>UNIT-4:Interfacing with 8051-Keyboard , seven segment display. (6H)           | Unit-5: DAC, ADC and Traffic light controller interfacing. PIC Micro controller- PIC 16F877,Features, pin diagram, Interfacing with LCD. (7H)<br><br>Internal test.                         |

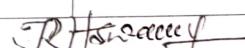
*W. Venkateswaran*  
**PRINCIPAL**  
**VIVEKANANDA DEGREE COLLEGE**  
**BENGALURU-55**

*R. H. S. Swamy*  
**K.M. Thipperudra Swamy**  
**HOD of Electronics**  
**Vivekananda Degree College**  
**Rajajinagar, Bangalore - 560 055**

**ACADEMIC PLANNER**  
**DEPARTMENT OF ELECTRONICS**  
**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR II STAGE, BENGALURU-55.**  
**NAME: Prof. Thipperudra Swamy K.M. HOD of Electronics.**  
**(I, III & V Semesters for the Academic Year 2018-19) Reopen – 02/07/2018**

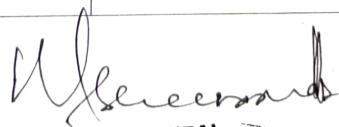
| Class         | July  | August  | September  | October   |
|---------------|---|---|--|---|
| I Sem B.Sc.   | <b>UNIT-1:</b> DC and AC response of Electronic passive components. (10H)<br><b>UNIT-2:</b> Networks Theorems (DC analysis) KCL, KVL, open and short circuits, Voltage and current divider theorems. (6H) | <b>UNIT-2:</b> Networks Theorems- Thevenin's, Norton's, and Superposition Theorems. (3H)<br><b>UNIT-3:</b> Semiconductor Diode and its applications-Zener diode Regulator, Transistor series regulator. (13H)<br>Internal Test. | <b>UNIT-4:</b> BJT and FET-Working, biasing, Characteristics, and amplifiers. (13H)<br><b>UNIT-5:</b> Number systems and Codes-Types of number systems and interconversion. (3H)         | <b>UNIT-5:</b> Number systems and codes- BCD, Gray, and excess-3 codes. ASCII and EBCDIC codes. Numerical problems. (9H)<br>Test and Assignments.                         |
| III Sem B.Sc. | <b>UNIT-3:</b> C Programming- Introduction, structure, operators, evaluation of expressions, Arrays, Programs. (8H)   | <b>UNIT-3:</b> Input and Output statements, library functions, programs. (4H)<br><b>UNIT-4:</b> Decision making, branching and looping- (4H)<br>Internal test.  | <b>UNIT-4:</b> for loop, do loop, while loop, function arguments and passing, programs. (4H)<br><b>UNIT-5:</b> Defining, declaring and initializing structure, arrays of structure. (4H) | <b>UNIT-5:</b> structure and functions, unions. Examples (4H)<br>Test and Assignments.  |
| V Sem B.Sc.   | <b>UNIT-1:</b> Introduction to Microprocessor- Features, different buses, addressing modes, Instruction set, T states, Delay oops, Numerical examples. (12H)  | <b>UNIT-2:</b> Stack operations, subroutine calls and returns, Assembly level Programs of various operations. Interrupts, and basic interfacing concepts. Internal test. (12H)  | <b>UNIT-3:</b> I/O instructions and Interfacing- Memory interfacing, i/o interfacing concepts, key board and LED interfacing. (2H)<br>Antennas: Full unit (8H)                           | <b>Unit-5:</b> Television- Introduction, Scanning, TV standards, monochrome TV transmitter and receiver, Color TV concepts and numerical problems. (8H)<br>Internal test. |

  
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**K.M. Thipperudra Swamy**  
**HOD of Electronics**  
**Vivekananda Degree College**  
**Rajajinagar, Bangalore - 560 055**

**ACADEMIC PLANNER**  
**DEPARTMENT OF ELECTRONICS**  
**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR II STAGE, BENGALURU-55.**  
**NAME: Prof. Thipperudra Swamy K.M. HOD of Electronics.**  
**(II, IV & VI Semesters for the Academic Year 2018-19) Reopen – 24/01/2019**

| Class        | January   | February  | March   | April   |
|--------------|---|---|---|---|
| II Sem B.Sc. | <b>UNIT-1:</b> Small Signal Amplifier-CE Amplifier, derivation for Av, Swamped Amplifier.<br><br>(4H) | Multistage Amplifier, Darlington Amplifier and JFET Amplifier. (8H)<br><b>UNIT-2:</b> Power and Tuned Amplifier-Classification, class A power amplifier, Class B push pull power Amplifier, tuned amplifiers. Internal test. (8H) | <b>UNIT-3:</b> Differential Amplifier- derivation for q point, Current mirror. (9H)<br><b>UNIT-4:</b> Concept, effect of -ve FB. Oscillators- Types, circuits, working and expressions . (9H) | Multivibrators, numerical problems. (3H)<br><b>UNIT-5:</b> MOSFET- Working & characteristics. UJT, SCR, LED and LCD – Construction, working and characteristics. (14H)                |
| IV Sem B.Sc. | <b>UNIT-1:</b> Boolean algebra, SOP & POS. Basic logic gates. (2H)                                    | Universal property of NAND & NOR Gates, K map, TTL NAND gate, CMOS inverter. (8H)<br>Internal test.   | <b>UNIT-2:</b> Combinational logic circuits-HA, FA, HS, FS, encoder, decoder, multiplexer, demultiplexer, A-D & D-A Conversion. Successive approximation ADC. (10H)                           | <b>UNIT-3:</b> Flip flops, Registers and counters. Design of synchronous counter using K Map. (8H)  |
| VI Sem B.Sc. | <b>UNIT-1:</b> Introduction to Microcontroller-Types, Architecture, Registers. (3H)                   | Memory organization of 8051, counters & timers, TCON, TMOD, SCON & PCON. (7H)<br><b>UNIT-2:</b> Interrupts, addressing modes, Data transfer instructions, Examples, (5H)  | Logical & arithmetic instructions, ALP. (5H)<br><b>UNIT-3:</b> Jump & Call instructions, simple programs. 8051 programming using C.(8H)<br>Internal test.                                     | <b>Unit-4:</b> Basic interfacing concepts, interfacing of 8051 to keyboard, stepper motor, DAC, ADC & Traffic light controller.<br>PIC Microcontroller- features & interfacing. (13H) |

  
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**Rajajinagar, Bangalore - 560 055**

## ACADEMIC PLANNER

VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55

Plan of Syllabus of Prof. Revanasiddappa. S. MasaliDepartment: Electronics

On-line classes: 01.09.2020

(I, III &amp; V Semesters, for the academic year- 2020-21.

On-line &amp; OFFLINE: 17.11.20 to 15.02.21.

December &amp; Jan, 2021

| Class         | September  | October   | November   | December & Jan, 2021   |
|---------------|--|---|--|--|
| I Sem B.Sc.   | ← Practical Classes →  |   |  |  |
| III Sem B.Sc. | OP Amp: Parameters. Characteristics of Ideal OPamp. -ve f.b in OP.Amp. Applications. Adder, Subtractor, Differentiator, Integrator. Derivation for Av.   | Small Signal amplifiers. O/p wave forms: Problems. Active Filters: Low-pass, High-pass, Band Pass and Band Reject filters: Derivation for O/p Voltage of L.P & H.P.               | Fixed & Variable Voltage regulators: IC 555 multivibrators, Ckt expn. Eqn for frequency of oscillations.   | Astable & Mono-stable Multivibrators. Revision of Unit 1&2 with previous papers. |
| V Sem B.Sc.   | Unit 1: Noise & T <sub>2</sub> line. Defn: Internal & External noise. Equivalent ckt: Primary & Secondary constants. VSWR. Losses in T <sub>2</sub> line. Wave propagation diagram of Superheterodyne. Unit 2: Analog Modulations. Am, FM & PM Derivation of Am wave frequency spectrum. | AM & FM modulators: Block diagram of AM & FM Transmitter. Transducers: Temp <sup>o</sup> Transducers. Photo-electric Transducers: MIC LVDT. Chopper, Carriers Lock-in amplifiers. | Unit 4: Instrumentation Instruments: Electrodes. Block diagram & expn of ECG & EEG. Unit 4: Antenna's. Power radiated. Radiation Pattern. Numerical Problem. |  |

R. Hanumanthu

( Revanasiddappa. S. Masali )

Ms BaluM. BeeraiahPRINCIPAL  
VIVEKANANDA DEGREE COLLEGE  
BENGALURU - 55

**ACADEMIC PLANNER**

VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55

Plan of Syllabus of Prof. Revanasiddappa. S. Masali. Department: Electronics.

(II, IV & VI Semesters, for the academic year- 2020 - 21.

Online classes: 03.05.2021 - 14.07.2021.  
Offline: 26.07.21 to 14.08.2021.

| Class        | April May   | May June   | June July   | July Aug.  |
|--------------|---|--|---|--|
| II Sem B.Sc. |   | Practicals - - - - -   |   |  |
| IV Sem B.Sc. | <u>Unit 1: Boolean Algebra and Logic gates</u> .<br>De-morgans Theorem SOP & POS. TTL Nand gate. TTL-IC Terminology. Half adder & Full Adder.       | <u>Unit 4: Introduction to Verilog</u> : History. Verilog module, Delays. Data flow, Behavioral, Structural & Mixed design Styles.   | Language Elements. Data types, Parameters Expressions: operators and Operands. Gate level modeling MOS switches. Examples.                                    | <u>Unit 5: Data - flow &amp; Behavioral Modeling</u> . Continuous assignment. Procedural Constructs. Procedural Assignment. Illustrative Examples. |
| VI Sem B.Sc. | Digital Communications: PAM, PWM, PPM & PCM. Digital Modulations. ASK, FSK, PSK. Modem modes of operation. Data Transmission Capacity of a Channel. | <u>Unit 2: Radar Range</u> : Pulse, MTI, CW & FM CW Radars. Block & exp12. <u>Unit 3: Satellite Comm.</u> Need, OSBTS, UP. Link & downlink Systems. Ground stations: TDMA & FDMA | <u>Unit 4: Optical Fibers</u> : Block diagrams, light propagation. Numerical aperture. Light sources. LED, Laser diode exp13. Losses in OFC. photo detectors. | <u>Unit 5: Cellular Communication &amp; wire less LAN</u> . Roaming frequency re-use, data encryption. 2G, 3G, 4G. Concepts. OSI-Model             |

R. S. Masali

P. H. Karan

M. Venkatesh

(Revanasiddappa.S. Masali).

**PRINCIPAL**  
**VIVEKANANDA DEGREE COLLEGE**  
**BENGALURU-55**

VIVEKANANDA DEGREE COLLEGE, BANGALORE -55  
MONTHLY REPORT OF ONLINE CLASSES FOR THE MONTH OF September, 2020.

Name of the Faculty: T. P. exudra Swamy: K.M

Department: Electronics.

Date: From: 01.09.2020

To: 30.09.2020

| Sl.No. | Date    | Time      | Class   | Section | Subject     | Topic/Basics discussed                      | Remarks |
|--------|---------|-----------|---------|---------|-------------|---|---------|
| 1      | 2/9/20  | 5 to 6 PM | III Sem | B       | Electronics | Introduction about online classes, zoom app |         |
| 2      | 3/9/20  | 6 to 7 PM | V Sem   | B       | —           | Introduction about syllabus contents        |         |
| 3      | 4/9/20  | 5 to 6 PM | III Sem | B       | —           | Discussion of syllabus contents             |         |
| 4      | 5/9/20  | 5 to 6 PM | V Sem   | B       | —           | Video clipping of MP basics                 |         |
| 5      | 7/9/20  | 5 to 6 PM | III Sem | B       | —           | Introduction to computers                   |         |
| 6      | 10/9/20 | 5 to 6 PM | V Sem   | B       | —           | Comparison and applications of MP & MC      |         |
| 7      | 11/9/20 | 5 to 6 PM | V Sem   | B       | —           | Types of microprocessors                    |         |
| 8      | 16/9/20 | 5 to 6 PM | III Sem | B       | —           | Introduction to computers continued         |         |
| 9      | 18/9/20 | 5 to 6 PM | III Sem | B       | —           | Introduction to computer languages          |         |
| 10     | 19/9/20 | 5 to 6 PM | V Sem   | B       | —           | Architecture of MP SOS                      |         |
| 11     | 21/9/20 | 5 to 6 PM | V Sem   | B       | —           | Architecture of MP Continued                |         |

T.P. exudra Swamy

Signature of the Faculty

R.H.S.f

Signature of the HoD

W. Meenakshi  
Principal  
**PRINCIPAL**  
**VIVEKANANDA DEGREE COLLEGE**  
**BENGALURU-55**

**VIVEKANANDA DEGREE COLLEGE, BANGALORE -55**  
**MONTHLY REPORT OF ONLINE CLASSES FOR THE MONTH OF .....September 2020.....**

**Name of the Faculty:** Thirupperudra Srinivasan K.M.

**Department:** Electronics

**Date:** From:...01-09-2020 To:...30-09-2020

RHS - f

### **Signature of the Faculty**

RHS

Signature of the HeD

## **Principal**

## ACADEMIC PLANNER

VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55

Plan of Syllabus of Prof. Revanasiddappa S. Masali. Department: ELECTRONICS.  
 (I, III & V Semesters, for the academic year- 2019 - 20.) Re-open: 08-07-2019.

| Class         | July  | August   | September  | October   |
|---------------|---|--|--|---|
| I Sem B.Sc.   | ← Practicals →  |  |  |   |
| III Sem B.Sc. | Operational amplifiers:<br>Block diagram, Parameters, characteristics, 3 different IC's.<br>Limitations of op. amp.<br>OP. Amp with -ve feedback<br>Inverting & Non-inverting<br>Derivation for Av.                                     | Apps of OP Amp: Adder, Subtractor, Diffr & Integrator.<br>Derivation for o/p voltage.<br>Scale Changer & Examples.<br>Waveform representation for Sine & Square waves.<br>Numerical Problems.  | Active Filters: Low pass, High pass, Band pass & Band reject Ckt's : Derivation for o/p voltage of L.P & H.P Filter.<br>Instrumentation amp.<br>Oscillators using OP-Amp.<br>Ckt & exptl of Wien-Bridge.   | Fixed & Variable Regulators<br>Oscillators (exptl).<br>o/p Voltage equation.<br>555 Timer as Astable, Monostable<br>multivibrator Ckt & exptl.<br>Eqn for frequency.    |
| V Sem B.Sc.   | Unit 1: Noise & T.R. lines:<br>Types, S/N & Noise figure<br>Numerical Problems.<br>T.R. lines: Primary & Secondary<br>constant, VSWR, CSWR defn.<br>Unit 2: Analog modulation.<br>AM, FM, PM. Derivation for<br>Am-wave freq. spectrum. | AM & FM Modulators:<br>Block diagram of AM & F.M. transmitters with AFC.<br>Pre-emphasis, Comparison.<br><br>Unit 3: Radio Receivers:<br>Diode & T.R. detectors: FM<br>detectors. Balanced slope detector.<br>Characteristics of Radio receiver. | Super-heterodyne Receivers.<br>Unit 4: Electronics Instrumentation: Characteristics.<br>Transducers: Active & Passive<br>Temp. Transducers, strain<br>gauges, photo electric trans<br>ducers, pressure transducers<br>Introduction to Bio-Medical<br>Instruments | Electrodes for ECG,<br>EEG & EMG.<br>Block diagram of<br>ECG & EEG exptl.<br>Unit 4: Antenna<br>Parameters: Derivation<br>for power radiated &<br>Radiation resistance. |

R. Hanseef

Practicals  
 (Revanasiddappa S. Masali)

Mr. Hanseef  
Principal  
 VIVEKANANDA DEGREE COLLEGE  
 BENGALURU-55

## ACADEMIC PLANNER

VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55

Plan of Syllabus of Prof. Revanasiddappa. S. Masali, Department: Electronics.

(II, IV &amp; VI Semesters, for the academic year- 2019 - 20. ) Re-open: 09.01.2020,

| Class        | January  | February  | March   | April / May.  |
|--------------|--|---|---|---|
| II Sem B.Sc. | ← - - - - -  | Practicals - - - - -  | - - - - -   | - - - - - →   |
| IV Sem B.Sc. | <u>Unit 1:</u> Boolean Algebra and logic gates; Boolean laws, DeMorgan's theorem, 3 & 4-Variable K-map. Numerical problems, classification of digital IC's. Characteristics. | <u>Unit 4:</u> Verilog: History, Structure of HPL Composision of HDL & VHDL, Verilog module switches, Bidirectional switches problems on Expressions, operators & operators. Built-in primitive gates. Illustrative exo. Language Elements. | Key words, Identifiers, Gate level modeling, MOS, switches, Bidirectional switches problems on Expressions, operators & operators. Built-in primitive gates. Illustrative exo.          | <u>Unit 5:</u> Data flow modeling & Behavioural Modeling: procedural constructs, loop statements, delays, net delays with examples. |
| VI Sem B.Sc. | <u>Unit 1:</u> Digital Commn: PAM, PWM, PPM & PCM, Digital Modulation; ASK, FSK, PSK, Digital Transmission Characteristics, Modern - Modes of Modern operation.              | <u>Unit 2:</u> RADAR Systems: Principle, Freq, pulse Radar Systems, Range Eqn., MTI, CW & FM CW Radar Block diagram, Numerical problem.<br><u>Unit 3:</u> Satellite-Commn, orbits, Satellite Sub System, Up link & Down link.               | C-Band Transponder, Path loss Problem, TDMA, FDMA, Comparison GPS services:<br><u>Unit 4:</u> Optical Fibers: Block diagram of OFC, light propagation, Derivation of Numerical aperture | Light source of OFC, LED, Photodiode, Losses in Fibers.<br><u>Unit 5:</u> Cellular Communication & wire less LAN.                   |

R. H. Masali

( Revanasiddappa. S. Masali )

M. Sheena  
PRINCIPAL  
VIVEKANANDA DEGREE COLLEGE

## ACADEMIC PLANNER

VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55

Plan of Syllabus of Prof. Revanasiddappa.S.Masali.

Department: Electronics.

(I, III &amp; V Semesters, for the academic year- 2018-19)

1) Re-open of I III/V Sem.  
02.07.2018.

| Class         | July  | August   | September   | October   |
|---------------|---|--|---|---|
| I Sem B.Sc.   |   |  |   |   |
| III Sem B.Sc. | ← Practicals →  |  |   |   |
| V Sem B.Sc.   | I) Noise & Transmission lines<br>Reflection Coefficient, Voltage Standing wave ratio, Prop. of waves<br>II) Analog Modulation Techniques, AM, FM, PM, Derivation of AM, Am & FM Modulators, Comparison, Am and FM generators, Varactor diode modulator. | <u>Unit 1:</u> Linear Integrated Ckts. OP.Amp: Adder, Subtractor, classification, Adv & dis. adv. Fabrication of Monolithic IC's Operational amplifiers: Parameters, characteristics, OP Amp with Negative feed back, Derivation for AV, Inverting & non-Inverting amplifiers. | <u>Unit 2:</u> Active Filters: low pass & high pass filters. Derivation for output voltage. Problems on L.P & H.P. Filter. Oscillators: Phase-shift, Wien-bridge, Ckt, & working. | Fixed & Variable IC Regulators: Op Voltage. Multivibrators: Astable & Monostable ckt diagram & expln. 555 IC-Timer Ckt & working. Problems. |

( Revanasiddappa.S.Masali )

R.S.D.F.HanrahanH.BelemanePRINCIPAL  
VIVEKANANDA DEGREE COLLEGE

## ACADEMIC PLANNER

VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55

Plan of Syllabus of Prof. Revanasiddappa. S. Masali, Department: Electronics.(II, IV & VI Semesters, for the academic year- 2018 - 19. ) Re-open: 24.01.2019.

| Class        | January  | February   | March  | April & May.   |
|--------------|--|--|--|--|
| II Sem B.Sc. | ← <u>Practicals</u> →  |  |  |  |
| IV Sem B.Sc. | <u>Unit 1:</u> Boolean Algebras<br>Logic gate: Boolean Laws.<br>Demorgan Theorem. SOP & POS.<br>K-map,         | 3 & 4 Variable K-map.<br>Numerical Problems.<br>Logic families, Classification<br>of digital IC's. Characteristics.<br><u>Unit 4:</u> Verilog: History, Struc-<br>ture of HDL Module. Comparison<br>Dataflow Style, Behavioral Style   | Structural & mixed design style<br>Expts with examples.<br>Language Elements: Key<br>words, Identifiers, real & strings.<br>Gate level modeling, MAS switches.<br>Bi-directional Switches.<br>Problems on Combinational clk. | <u>Unit 5:</u> Dataflow<br>modeling and<br>Behavioral modell.<br>Continuous assignment<br>Timing Control.<br>Illustrative Examples.  |
| VI Sem B.Sc. | <u>Unit 1:</u> Digital Commn.<br>PAM, PWM, PPM & PCM.<br>Digital Modulation.<br>ASK, FSK, PSK characteristics. | Data Transmission: Capacity of a<br>Channel. <u>Modem</u> : Classification.<br><u>Unit 2:</u> RADAR: Range Eqn.,<br>Pulse, MTI & CWT, FMcw Radar<br>Block diagram & explain.<br><u>Unit 3:</u> Satellite Commn.:<br>Orbits, need, space segment<br>Uplink & Down link, C-Band. | Pathloss, effect of ground.<br>TDMA, FDMA CDMA Concept.<br>GPS-Services<br><u>Unit 4:</u> Optical Fibers:<br>Need, light propagation.<br>Numerical-aperture (NA).<br>Light Sources, LED, Laser diode<br>Photo detectors.     | Losses in Fibers.<br><u>Unit 5:</u> Cellular<br>Communication.<br>Concept, Freq reuse<br>Cell splitting. Roaming.<br>CDMA Technology.<br>2G, 3G, 4G concepts.<br>LAN, OST model. |

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( Revanasiddappa. S. Masali )

R. H. Hasan  
(AO)N. M. Greenoak  
PRINCIPAL  
VIVEKANANDA DEGREE COLLEGE

## ACADEMIC PLANNER

**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55**

**Plan of Syllabus of Prof. Thipperturda Swamy, K.M**      Department: Electronics

( II, IV & VI Semesters, for the academic year- 2017 -18 ) Reopen - 22/01/2018

| Class        | January  | February  | March  | April  |
|--------------|--|---|--|--|
| II Sem B.Sc. | <u>Unit 1</u><br>classification of amplifiers<br>CE amplifier, Derivations for Av. Expressions for Zi & Zo | <u>Unit 1</u> - multistage amplifiers<br>JFET amplifiers.<br><u>Unit 2</u> : Power and tuned amplifier          | <u>Unit 3</u> : Differential amplifier<br><u>Unit 4</u> : Feedback, Voltage Series feedback, Sinusoidal oscillators.               | <u>Unit 4</u> :<br>Multivibrators<br><u>Unit 5</u> :<br>Special purpose circuits.  |
| IV Sem B.Sc. | <u>Unit 1</u> : Introduction about digital Signal and circuits   | <u>Unit 2</u> : combinational logic circuits<br>cepto demultiplexer using gates                                 | D/A + A/D conversion<br><u>Unit 3</u> : Sequential logic circuits - cepto flip-flop  | <u>Unit 3</u> : Registers and counters<br>PCDS.                                    |
| VI Sem B.Sc. | <u>Unit 1</u> : Introduction to Microcontroller  | <u>Unit 1</u> : Microcontroller 8051 - architecture<br>Registers<br><u>Unit 2</u> :- Interrupt addressing modes | <u>Unit 2</u> : Data transfer and arithmetic instructions<br><u>Unit 3</u> : 8051 programming in C, Timer and counter programming. | <u>Unit 4</u> : Interfacing with 8051 and<br><u>Unit 5</u> :- PIC microcontrollers |

D. H. Swamy  
HOD

M. Bhagavath  
**PRINCIPAL**  
**VIVEKANANDA DEGREE COLLEGE**  
**BENGALURU-55**

R. Haranayya  
M. Thipperturda Swamy  
HOD of Electronics,  
Vivekananda Degree College  
Rajajinagar, Bangalore-560 053

**ACADEMIC PLANNER**

**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55**

**Plan of Syllabus of Prof. Revanasiddappa. S. Masali**

**Department: ELECTRONICS.**

**( II, IV & VI Semesters, for the academic year-**

**2017 - 18 ) Reopen : 22.01.2018 .**

| Class        | January   | February  | March   | April  |
|--------------|---|---|---|--|
| II Sem B.Sc. | ←<br>Practicals →   |   |   |  |
| IV Sem B.Sc. | <u>Unit 1:</u> Boolean Algebra<br>Boolean Laws De morgan's theorem. SOP, POS. K-map. 3&4 Variables. numerical examples.   | <u>Unit 1:</u> Continued: Logic families, classification of Digital IC's, characteristics.<br><u>Unit 4:</u> Verilog: Brief History, Structure of HDL module. Comparison of Verilog & VHDL.   | <u>Verilog:</u> Delay, Dataflow style, Expressions, Behavior Style, Structural & Mixed Design Style. Simulating Design.<br><u>a</u> Language elements: Key words, Identifiers, format, real & string.<br><u>b</u> Built-in primitive functions<br><u>c</u> Dataflow & Behavior modeling Examples. | ④ Expressions, Operand & operators, Gate level modeling, Built-in primitive functions, Behavioral modeling Examples.   |
| VI Sem B.Sc. | <u>Unit 1:</u> Digital Commn. PAM, PDM, PPM, PCM. Digital modulation ASK, FSK, PSK, Characteristics of Data transmission. Capacity of channel, noise, cross talk, echo suppressors. Modems: Classification. | <u>Unit 2:</u> RADAR: Frequency Derivation of Range Eqn. Pulse Radar, MTI, CW and FM CW Radar Block & expln.<br><u>Unit 3:</u> Satellite Commn, orbits. Adv. of Geo-stationary orbit. Block diagram of satellite sub-systems. Up-link, downlink | C-band Satellite Transponder. TDMA, FDMA, CDMA. expln GPS services, SPS, & PPS.<br><u>Unit 4:</u> Optical fiber Commn, need, OFC cable, Light propagation through OFC, Light sources. LED & Laser diode Construction & working  | PIN - photo diodes & Avalanche Photo diode LOSSES. Advantages, Losses. Cellular Communications: SIM Card - IMEI No. Block of cellular Hand Set GSM, GPRS, 2G, 3G, 4G, GPRS, LAN, Wi-Fi, GPRS, etc. |

Rev.  
R. S. Masali

( Revanasiddappa. S. Masali )

M. Gleason  
PRINCIPAL  
VIVEKANANDA DEGREE COLLEGE  
BENGALURU-II-55

R. Horace  
Vice Principal  
HOD of Electronics  
Vivekananda Degree College  
Bengaluru-II-55

## ACADEMIC PLANNER

**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55**

**Plan of Syllabus of Prof. Revanasiddappa. S. Masali**

**Department: ELECTRONICS.**

( II, IV & VI Semesters, for the academic year- 2017-18 ) Reopen : 22.01.2018 .

| Class        | January  | February  | March  | April   |
|--------------|--|---|--|---|
| II Sem B.Sc. | ←<br>Practicals →  |   |  |   |
| IV Sem B.Sc. | <u>Unit 1:</u> Boolean Algebra<br>Boolean Laws De Morgan's theorem. SOP, POS. K-map. 3&4 Variables. numerical Examples.  | <u>Unit 2:</u> Continued: Logic families, classification of Digital IC's, characteristics.<br><u>Unit 3:</u> Verilog: Brief History, Structure of HDL module. Comparison of Verilog & VHDL.   | <u>Verilog:</u> Delay, Dataflow style, Expressions. Behavior Style, Structural & Mixed Design Style. Simulating Design.<br><u>a</u> Language elements: Key words, Identifiers, format, real & strings. | ② Expressions.<br>Operand & operator<br>Gate level modeling.<br>Builtin primitive gate<br>units.<br>Data flows<br>Behavior modeling<br>Examples.  |
| VI Sem B.Sc. | <u>Unit 1:</u> Digital Commn. PAM, PDM, PPM, PCM. Digital modulation ASK FSK, PSK, Characteristics of Data transmission. Capacity of Channel, noise, cross talk, echo suppressors. Modems: Classification. | <u>Unit 2:</u> RADAR: Frequency Derivation of Range Eqn. Pulse Radar, MTI, CW and FM CW Radar Block & expln.<br><u>Unit 3:</u> Satellite Commn., orbits. Adv. of Geo-stationary orbit. Block diagram of satellite sub-systems. Up-link, down-link | C-band Satellite Transponder. TDMA, FDMA, CDMA. expln GPS services, SPS, & PPS.  | PIN - photo diode<br>Avalanche photo diode<br>Losses. Advantages<br><u>Unit 4:</u> Optical fiber Commn. need, OFC cable, Light propagation through OFC, Light sources. LED & Laser diode Construction & working |

Revanasiddappa. S. Masali

W. S. Masali  
**PRINCIPAL**  
**VIVEKANANDA DEGREE COLLEGE**  
**BENGALURU-55**

R. Hosseley  
K.M. Thippendra-Swamy  
HOD of Electronics,  
Vivekananda Degree College,  
Rajajinagar, Bengaluru-55

## ACADEMIC PLANNER

**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55**

**Plan of Syllabus of Prof. K. M. Thippeswamy.**

**Department: ELECTRONICS.**

**Re-opening: 02.01.2017. (II, IV & VI Semesters, for the academic year- 2016-17 )**

| Class  | January  | February   | March   | April  |
|--|--|--|---|--|
| <b>II Sem B.Sc.<br/>Electronic Circuits &amp; Special Purpose devices.<br/>EL-201T</b> | <u>Unit 1:</u> Small Signal amplifiers: Classification CE amplif. derivation of AV. Zin & Zout - Multistage amplif. RC-coupled, direct Coupled-JFET- Amplif. ckt operation expression for Voltage gain Numerical problems: 12(Hrs) | <u>Unit 2:</u> Power and Tuned amplifiers. CLASS A, B, C, Push pull, class B push pull. Tuned amplif - Single & double (9 Hrs)   | <u>Unit 3:</u> Current mirrors: differential amplif with current mirror. (4 Hrs) <u>Unit 4:</u> Feed back oscillators. effect of -ve f.b. Zif, ZD & B.W. Sinusoidal oscillators Hartley & Colpitts oscillators. Multivibrators: Monostable, Astable working. (12 Hrs) | <u>Unit 5:</u> Special purpose devices. MOSFET. UJT, SCR, LED, LCD. Tunnel diode, Varactor diode. 7-segment display. (14 Hrs)                  |
| <b>IV Sem B.Sc.<br/>Digital Electronics &amp; Verilog.<br/>EL-401T</b>                 | <u>Unit 1:</u> Boolean Algebra and logic gates. K-map- 3 & 4-Variable. TTL IC's terminology. CMOS inverter, Combinational (10 Hrs)   | <u>Unit 2:</u> Combinational logic Circuits: half & full adder Subtractor, BCD to decimal de Coder. BCD to 7 segment decoder. MUX: 4:1 & Demux. D-A Converter R-2 R ladder A-D conversion 10 Hrs                                       | <u>Unit 3:</u> Sequential logic Circuits: RS-latch. D-FF JK FF, Registers & counters. ASynchronous Counter. 4-bit Serial & Parallel Counter. 3 bit up-down counter. (8 Hrs)   | Synchronous Counter design using K-map. Programmable logic devices. Types of PLDS mention. (4 Hrs)   |
| <b>VI Sem B.Sc.<br/>Micro-Controllers<br/>EL-602T</b>                                  | <u>Unit 1:</u> Introduction to micro-Controller. MC-8051 Architecture, Key features of 8051. (10 Hrs)<br><u>Unit 2:</u> 8051- Interrupts, Addressing mode & Instruction set (4 Hrs)  | <u>Unit 3:</u> Data transfer instructions: Logical instructions. Arithmetic instructions. (6 Hrs)<br><u>Unit 4:</u> 8051 programming inc. Jump & call instructions. 8051 programming: I/o programs, Timer/Counter programming. (9 Hrs) | <u>Unit 4:</u> Interfacing with 8051: Basic Concepts. Interfacing of 8051 to Key board, Seven segment display, Stepper motor, DAC, ADC & traffic light Controller etc. (9 Hrs)  | <u>Unit 5:</u> PIC - Micro Controllers: Core features, overview of PIC micro. PIC-16F877 A-features, Pin diagram, interfacing with LCD (4 Hrs) |

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**BENGALURU-55**

  
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98452 03355

## ACADEMIC PLANNER

**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55**

**Plan of Syllabus of Prof. Revanasiddappa. S. Masali.**

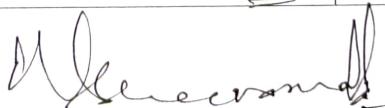
**Department: ELECTRONICS.**

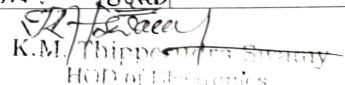
**( II, IV & VI Semesters, for the academic year-**

**2016 - 17. )**

| Class  | January  | February   | March   | April  |
|--|--|--|---|--|
| II Sem B.Sc.   | —  | —  | —   | —  |
| IV Sem B.Sc.<br>Digital<br>Electronics<br>&<br>Verilog | <u>Unit 4:</u> Introduction to Verilog : History of HDL, module, simulation, Verilog module, Delay, data flow state, Behavioral structural mixed design, Language elements (7 hrs)                           | 4) Expressions: operand & operators, types of expressions. Gate level modeling: Built-in Primitive gates: Examples. Combinational & Sequential logic Circ. (15m)   | <u>Unit 5:</u> Data flow modeling and Behavioral " . Continuous assignment, net declaration assignment, delay net delay & examples. (6 hrs)   | 5) Behavioral modeling: Procedural Constructs timing Controls. Block Statements. Illustrative examples. (5 hrs)        |
| VI Sem B.Sc.<br>Communcation<br>II.                    | <u>Unit 1:</u> Digital Comm.: PAM, PWM, PPM, ASK FSK, PSK, Digital transmission modems - classification (8 hrs)<br><u>Unit 2:</u> Radar- Systems, Freq & power used, Radar range equation derivation (5 hrs) | 2) MTI Radar, CW Radar & FM CW Radar Blocks & expln. numerical example (5 hrs)<br><u>Unit 3:</u> Satellite Comm.: Orbit, Block diagram of satellite Sub system, C-band, TDMA, FDMA & CDMA. GPS - services. (8 hrs) | <u>Unit 4:</u> Optical Fiber Communication : Block diagram, Light propagation derivation for NA & O. Losses, Adv & Dis advantage. light sources. (9 hrs)<br><u>Unit 5:</u> Cellular Comm & wireless LAN: (10 hrs) | 5) Local Area network OSI-model, Concept of Blue-tooth, Wi-Fi & wi max. CDMA, Comparative study of GSM & CDMA (10 hrs) |

  
**(R.S. masali)**  
 Sign. of the Teacher.

  
**M. Bleecanada**

  
**K.M. Thippeswamy**  
 HOD of Electronics  
 Vivekananda Degree College  
 Rajajinagar, Bengaluru-557

# ACADEMIC PLANNER

**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55**

**Plan of Syllabus of Prof. K. M. Thipperudra Swamy**

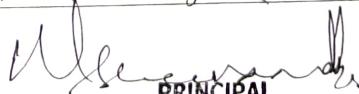
**Department: ELECTRONICS**

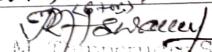
**(I, III & V Semesters, for the academic year- 2016-17 )**

| Class                                     | July  | August  | September   | October   |
|---|---|---|---|---|
| I Sem B.Sc.<br>Basic Electronics<br>I     | <u>Unit 1:</u> D.C & A.C. response of Passive Components: RC & RL CKts. AC applied to RC & RL CKts. Series & parallel RL CKts. Transformer, Principle, Conn'tn. Switcher, fuse, Relay - (10 hrs)  | <u>Network theorems:</u> Thevenin, Norton, Superposition, Reciprocity. Steps involved. Max power transfer theorem. Problems. (10 hrs)<br><u>Unit 3:</u> Semiconductor diodes & applications, PN-junction. Rectifiers, Filter type CKts. Zener diode regulators. Transistor Series Regulator. (10 hrs) | <u>Unit 4:</u> BJT and FET Construction, CE, CB, CC. Details of $\alpha$ , $B$ & $\beta$ . Study of CE & CB characteristics. h-parameter. Ty Biasing. Types, exp'n. T as switch. JFET Construction & working. FET parameter: (13 hrs) | <u>Unit 5:</u> Number Systems & Codes. Binary, hexa, Octal & Vice-versa Sub-coding & Complement. BCD Codes. Gray & excess-3 Code. Self Complementing Property. (12 hrs) |
| III Sem B.Sc.<br>Linear IC's & C. program | <u>Unit 3:</u> C programming. Key words, identifiers, Convents & datatype. Arithmetic operators, Array concepts. S/n, O/P statements. Print(), Scan() & getch(). & library functions (12 hrs)   | <u>Unit 4:</u> Decision Making, Branching and looping. if- else if- else, switch statement, function arguments and passing, returning values (8 hrs)  | <u>Unit 5:</u> Structures and Unions: defining & declaring a structure, copying & comparing structure. Variable Array, Union size, example programs. (8 hrs)  | -   |
| V Sem B.Sc.<br>MP & Instruments.          | <u>Unit 1:</u> Introduction to MP. Basic block diagram, Speed wordsize, memory size. MP- 8085: Architecture internal registers, flag. stack pointer, progr. Counter. 8085- instructions Operation Code, Immediate, machine Control. (9 hrs) | <u>Unit 2:</u> Stack operations of MP- Prog programming. Programs for data transfer, addition & subtraction of 8 & 16 bits multiplication, storing, no of 1's & 0's, testing for zero condition. N-byte nos. progr. to find GCD of two integers! (8 hrs)  | <u>Unit 3:</u> I/O instructions and Interfacing. Basic, compatible I/O. LED display interfacing PPI IC - 8255 (8 hrs)   | <u>Unit 5:</u> Bio-medical instruments: origin ECG, EEG & EMG. Block diagrams & exp'n: electrode for the above. (8 hrs)   |

K.M. Thipperudra Swamy

  
K. M. Thipperudra Swamy,  
Electronics,  
Vivekananda Degree College  
Rajajinagar, Bangalore-55  
Date: 10/07/2016

  
**PRINCIPAL**  
**VIVEKANANDA DEGREE COLLEGE**  
BENGALURU-55

  
K.M. Thipperudra Swamy  
Principal  
Vivekananda Degree College

Rajajinagar, Bangalore-55  
Date: 10/07/2016

**ACADEMIC PLANNER**

**VIVEKANANDA DEGREE COLLEGE, RAJAJINAGAR-II STAGE, BENGALURU-55**

**Plan of Syllabus of Prof. Revanasiddappa. S. Masali, Asso. Prof. Department: ELECTRONICS**

( I, III & V Semesters, for the academic year- 2016-17. )

| Class   | July   | August  | September   | October   |
|---|--|---|---|---|
| I Sem B.Sc.   | -  | -   | -   | -   |
| III Sem B.Sc.<br>Linear<br>Integrated<br>Circuits<br>&<br>C programming | <u>Unit 1:</u> Integrated Circuits and - Operational Amplifiers. Classification, terminology, OP-Amp's: Parameters. IC-741, types: LM308, OP-07. Comparisons. Open-loop mode. OP-amp with -ve f.b. (9+12)  | 1) Derivation for Av, Adder, Sub, Average amp.<br>Integrator & differentiator.<br>Square signal half wave rectified + bias.<br><u>Unit 2:</u> Applications of operational amplifiers and IC 555. Open loop applications. (6+12)   | 2) First order Active Filters. Lowpass/high-pass, derivation for cut off freq & problems. Phase-shift & Wien bridge oscillator using OP-Amp. Fixed & Variable IC-regulators. LM-317. (6+12) | 3) 555-Timers: functional diagram, A stable multivibrator. 555 timers working. ESR for freq of oscillation. Mono-stable multiv. (4+12)                  |
| V Sem B.Sc.<br>Communi-<br>cation<br>I.                                 | <u>Unit 1:</u> Noise & Transmission lines: internal, external noise figure, Tr line reflection co-efficient, sky wave (7+12)<br><u>Unit 2:</u> Analog Modulation. Am, Fm, Pm, derivation power relation Am collector modulator. Limitation of Am & Fm (5+12) | 2) FM: Freq. spectrum, B.W. freq. deviation. Fm generators, Block diagram FM transmitter, Pre- & de-emphasis. (5+12)<br><u>Unit 3:</u> Radio Receivers; Linear diode detector, Fm detector, Fm super heterodyne, qualitative study of sensitivity, selectivity, g.r.t., | <u>Unit 4:</u> Antennas: Radiation mechanism, Directive gain, power gain, B.W & Beam width. Derivation for power radiated by antenna. Numerical problems. (8+12)                            | <u>Unit 5:</u> Television: Scanning: blanking & synchronizing pulses. TV Transmitter and Receiver, colour TV, primary & secondary colours. CCTV. (8+12) |

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